6223A-SRD

Wi-Fi Single-band 1X1 + Bluetooth 2.1/4.2

Combo Module Datasheet

6223A-SRD Module Datasheet

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Customer Approval : _____ Company

_____ Title

_____ Signature

_____ Date

_____ Fn-Link

Revision History

Version	Date	Revision Content	Draft	Approved
1.0	2018/10/16	New version	Lzm	Jacky
1.1	2018/12/18	Modify the telephone number	Lzm	Lxy
1.2	2018/12/25	Modify the office and TEL	Lzm	Lxy
1.3	2019/01/08	Add Carrier Tape Detail	Lzm	Lxy
1.4	2019/01/24	Update pin outline	WHH	Lxy
1.5	2019/03/07	Update material list match with bom	WHH	Lxy
1.6	2019/09/17	Update dimension information	Lxy	Szs
1.7	2020/08/04	add the description of 7th pin	Fc	Lxy
1.8	2020/09/17	Update BT power	Lxy	Szs
1.9	2020/10/30	Update reflow peak temperature	Lxy	Szs
2.0	2021/4/10	Added PCM interface information Remove confidential statement	Lxy	Szs
2.1	2021/5/21	Updata TX criteria for 美的	Lxy	Szs
2.1	2021/7/28	modify mimo to siso	Lxy	QJP

CONTENTS

1 Overview

1.1 Introduction

6223A-SRD is a small size and low profile of Wi-Fi + BT Combo module with LGA (Land-Grid Array) footprint, board size is 12mm*12mm. It can be easily manufactured on SMT process and highly suitable for tablet PC, ultra book, mobile device and consumer products. It provides SDIO interface for Wi-Fi to connect with host processor and high speed UART interface for BT. It also has a PCM interface for audio data transmission with direct link to external audio codec via BT controller. The Wi-Fi throughput can go up to 150Mbps in theory by using 1x1 802.11n b/g/n SISO technology and Bluetooth can support BT2.1and BT4.2.

6223A-SRD uses highly integrated Wi-Fi/BT single chip based on advanced COMS process. 6223A-SRD integrates whole Wi-Fi/BT function blocks into a chip, such as SDIO/UART, MAC, BB, AFE, RFE, PA, EEPROM and LDO/SWR, except fewer passive components remained on PCB.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

1.2 Features

- Operate at ISM frequency bands (2.4GHz)
- SDIO for Wi-Fi and UART for Bluetooth
- IEEE standards support: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n, IEEE 802.11d, IEEE 802.11e, IEEE 802.11h, IEEE 802.11i
- Compatible with Bluetooth 2.1+EDR and V4.2 systems
- Support Bluetooth 4.0 Dual mode
- Full–speed Bluetooth operation with Piconet and Scatternet support
- PCM interface for audio data transmission via BT controller
- Enterprise level security which can apply WPA/WPA2 certification for Wi-Fi.
- Wi-Fi 1 transmitter and 1 receiver allow data rates supporting up to 150 Mbps downstream and 150 Mbps upstream PHY rates

1.3 General Specification

Model Name	6223A-SRD
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x2.1 (typical) mm
Wi-Fi Interface	Support SDIO V2.0
BT Interface	UART / PCM
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 85°C
RoHS	All hardware components are fully compliant with EU RoHS directive

1.4 Recommended Operating Rating

The digital IO supports VDD33 or VDD18 application.

	Min.	Typ.	Max.	Unit
Operating Temperature	0	25	70	deg.C
VCC33	3.15	3.3	3.45	V
VDDIO	1.7	1.8 or 3.3	3.45	V

※1.5 EEPROM Information

WI-FI

Vendor ID	024C
Product ID	D723

2 Wi-Fi/BT RF Specification

2.1 2.4GHz RF Specification

Feature	**Description**			
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant			
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)			
Number of Channels	2.4GHz：Ch1 ~ Ch14			
Test Items	**Typical Value**			**EVM**
Output Power[1]	802.11b /11Mbps : 17dBm ± 1.5 dB			EVM ≤ -10dB
	802.11g /54Mbps : 15dBm ± 1.5 dB			EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 1.5 dB			EVM ≤ -28dB
Spectrum Mask	Min. b/g/n	Typ. b/g/n	Max. b/g/n	Unit b/g/n
1st side lobes(to fc ± 11MHZ)	-	-42/-38/-32	-	dBr
2st side lobes(to fc ± 22MHZ)	-	-52/-60/-60	-	dBr
Freq. Tolerance	-20/-20/-20	-	20/20/20	ppm
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps	PER @ -91 dBm		≤-83
	- 2Mbps	PER @ -89 dBm		≤-80
	- 5.5Mbps	PER @ -86 dBm		≤-79
	- 11Mbps	PER @ -84 dBm		≤-76
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps	PER @ -87 dBm		≤-85
	- 9Mbps	PER @ -86 dBm		≤-84
	- 12Mbps	PER @ -84 dBm		≤-82
	- 18Mbps	PER @ -82 dBm		≤-80
	- 24Mbps	PER @ -79 dBm		≤-77
	- 36Mbps	PER @ -75 dBm		≤-73
	- 48Mbps	PER @ -71 dBm		≤-69
	- 54Mbps	PER @ -70 dBm		≤-68
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -87 dBm		≤-85
	- MCS=1	PER @ -84 dBm		≤-82
	- MCS=2	PER @ -82 dBm		≤-80
	- MCS=3	PER @ -79 dBm		≤-77
	- MCS=4	PER @ -75 dBm		≤-73
	- MCS=5	PER @ -71 dBm		≤-69
	- MCS=6	PER @ -70 dBm		≤-68

	- MCS=7 PER @ -69 dBm	≤-67
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0, PER @ -84 dBm	≤-82
	- MCS=1, PER @ -81 dBm	≤-79
	- MCS=2, PER @ -79 dBm	≤-77
	- MCS=3, PER @ -76 dBm	≤-74
	- MCS=4, PER @ -72 dBm	≤-70
	- MCS=5, PER @ -68 dBm	≤-66
	- MCS=6, PER @ -67 dBm	≤-65
	- MCS=7, PER @ -66 dBm	≤-64
Maximum Input Level	802.11b : -8 dBm	
	802.11g/n : -20 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

1. HT40 MCS7 and 11M mode power calibrated by module side,other rate power control by firmware driver.

2.2 Bluetooth Specification

Feature	**Description**		
General Specification			
Bluetooth Standard	Bluetooth V4.2 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, π/4-DQPSK, 8-DPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power (Class 1)	2	5	8 dBm
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-89 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-83 dBm	

Maximum Input Level	GFSK (1Mbps):-20dBm
	π/4-DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

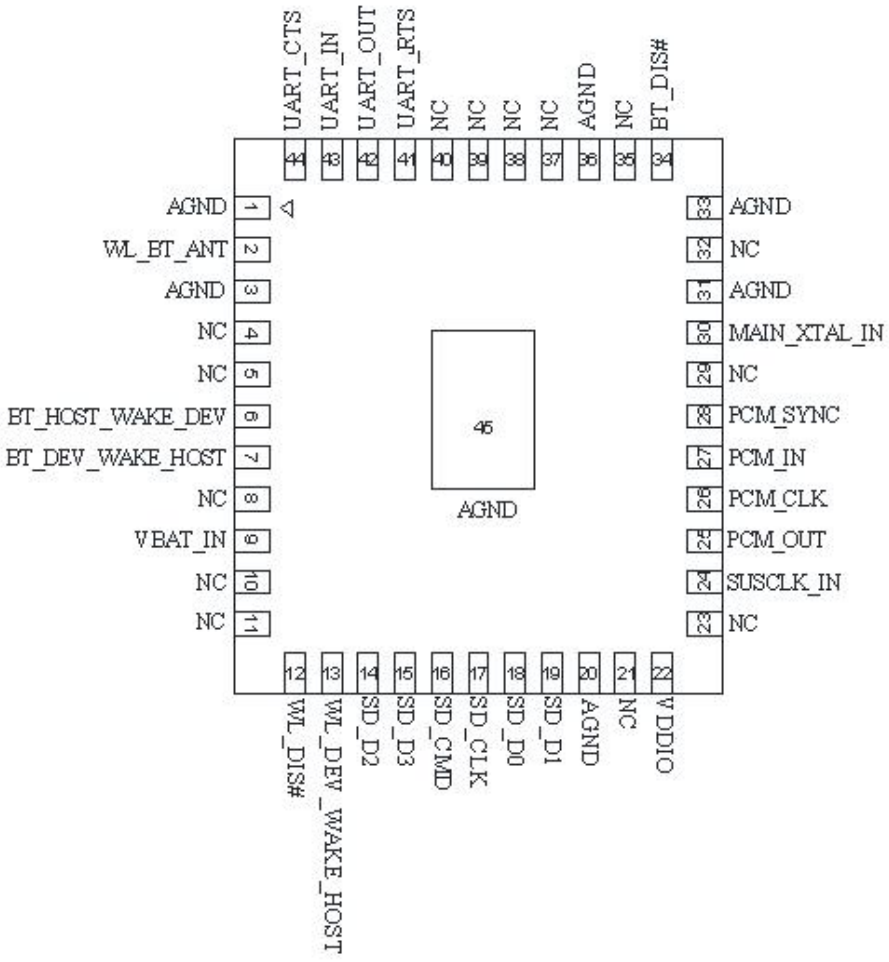
3 Power Consumption

Power Consumption (Typical by using SWR)	Wi-Fi only: TX n mode 40MHz: 133 mA RX n mode 40MHz: 53 mA TX n mode 20MHz: 137 mA RX n mode 20MHz: 47 mA

4 Pin Assignments

4.1 Pin Outline

< TOP VIEW



4.2 Pin Definition

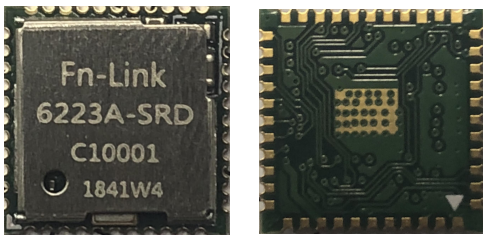
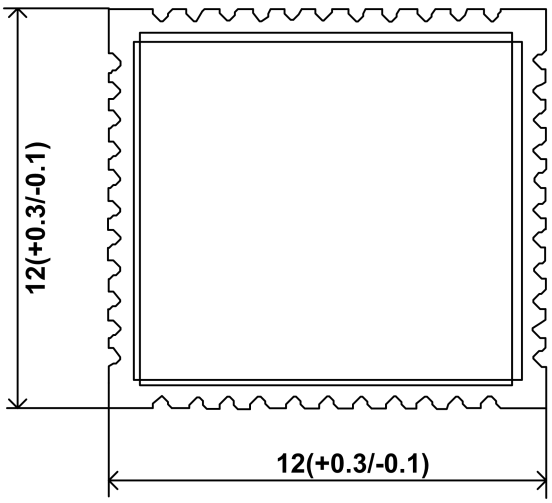
NO.	Name	Type	Description	Voltage
1	AGND		Ground connections	
2	WL_BT_ANT	I/O	RF I/O port	
3	AGND		Ground connections	
4	NC		Floating (NC)	
5	NC		Floating (NC)	
6	HOST_WAKE_BT	I	Host to wake up Bluetooth device	VDDIO
7	BT_WAKE_HOST	O	Bluetooth device to wake up host. (muti function for Test mode configuration. pull high to test mode ; pull low to normal mode .when wifi power on this pin must keep low)	VDDIO
8	NC		Floating (NC)	
9	VBAT_IN	P	3.3±10% V Main power voltage source input	3.3V
10	NC		Floating (NC)	
11	NC		Floating (NC)	
12	WL_DIS#	I	Pull high: ON , Pull low: OFF External pull low can disable WL	3.3V
13	WL_HOST_WAKE	O	WLAN to wake up HOST	VDDIO
14	SD_D2	I/O	SDIO data line 2	
15	SD_D3	I/O	SDIO data line 3	
16	SD_CMD	I/O	SDIO command line	
17	SD_CLK	I	SDIO clock line	
18	SD_D0	I/O	SDIO data line 0	
19	SD_D1	I/O	SDIO data line 1	
20	AGND		Ground connections	
21	NC		Floating(NC)	
22	VDDIO	P	I/O Voltage supply input	VDDIO
23	NC		Floating (NC)	
24	SUSCLK_IN	I	External Clock input(32.768kHz). Can keep NC.	
25	PCM_OUT	O	PCM Output	VDDIO
26	PCM_CLK	I/O	PCM Clock	VDDIO
27	PCM_IN	I	PCM Input	VDDIO
28	PCM_SYNC	O	PCM Sync	VDDIO
29	NC		Floating (NC)	

30	MAIN_XTAL_IN	O	Floating (NC)	
31	AGND		Ground connections	
32	NC		Floating (NC)	
33	AGND		Ground connections	
34	BT_DIS#	I	Pull high: ON , Pull low: OFF External pull low can disable BT	3.3V
35	NC		Floating (NC)	
36	AGND		Ground connections	
37	NC		Floating (NC)	
38	NC		Floating (NC)	
39	NC		Floating (NC)	
40	NC		Floating (NC)	
41	UART_RTS		UART RTS, module side is Ground connections	
42	UART_OUT	O	UART Output	VDDIO
43	UART_IN	I	UART Input	VDDIO
44	UART_CTS	I	UART CTS,	VDDIO
45	AGND		Floating (NC)	

P:POWER I:INPUT O:OUTPUT VDDIO:3.3V

5 Dimensions

5.1 Module Picture

<table>
<tr><td>L x W : 12 x 12 (+0.3/-0.1) mm
 
</td><td> 
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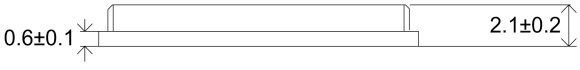
<tr><td>H: 2.1 (±0.2) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>0.54g</td></tr>
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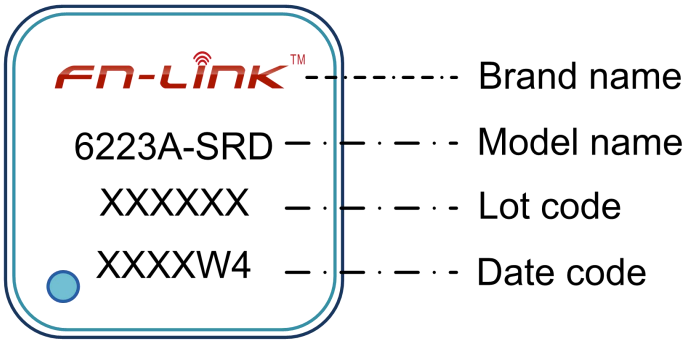
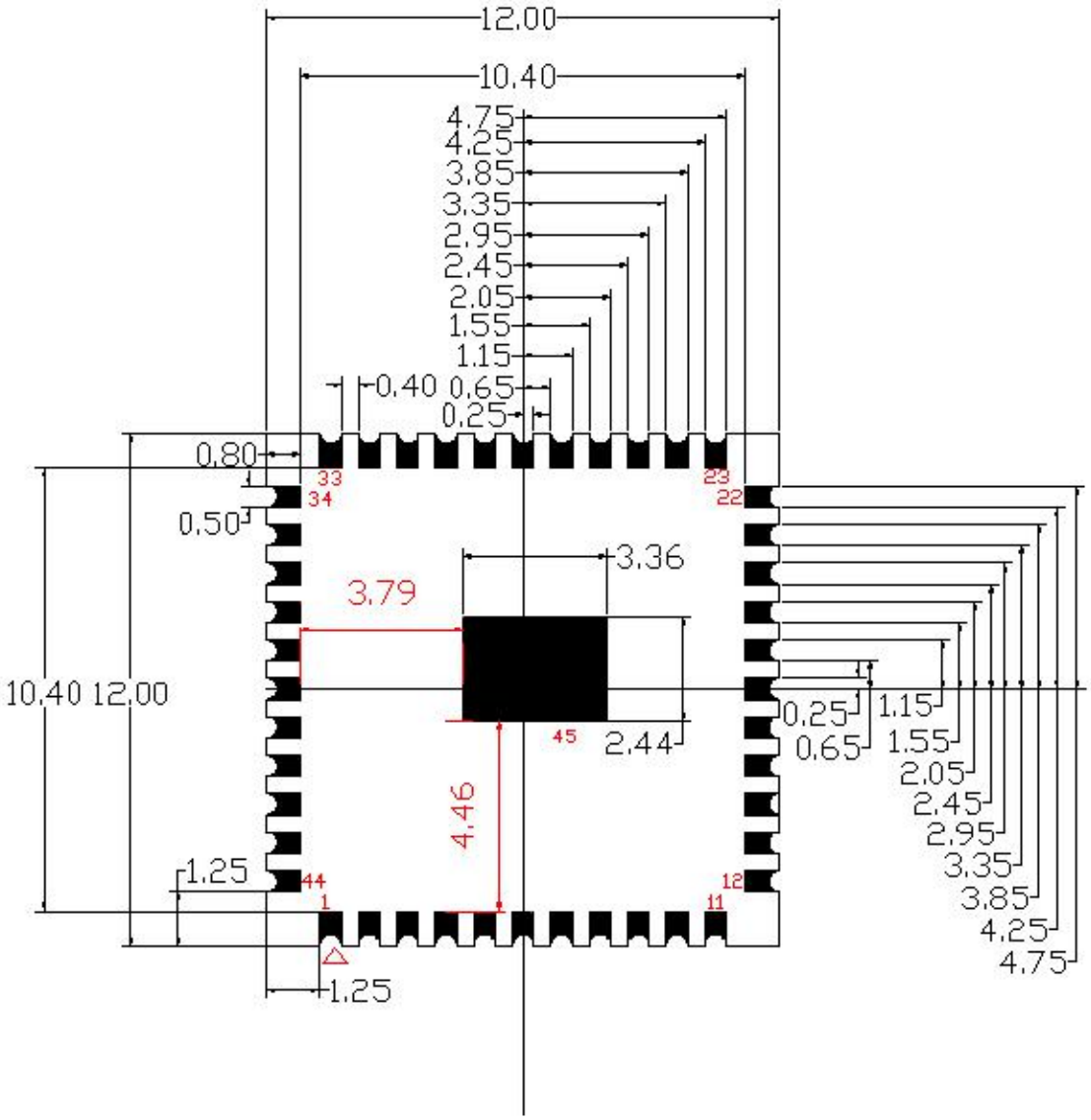
5.2 Marking Description

< TOP VIEW >

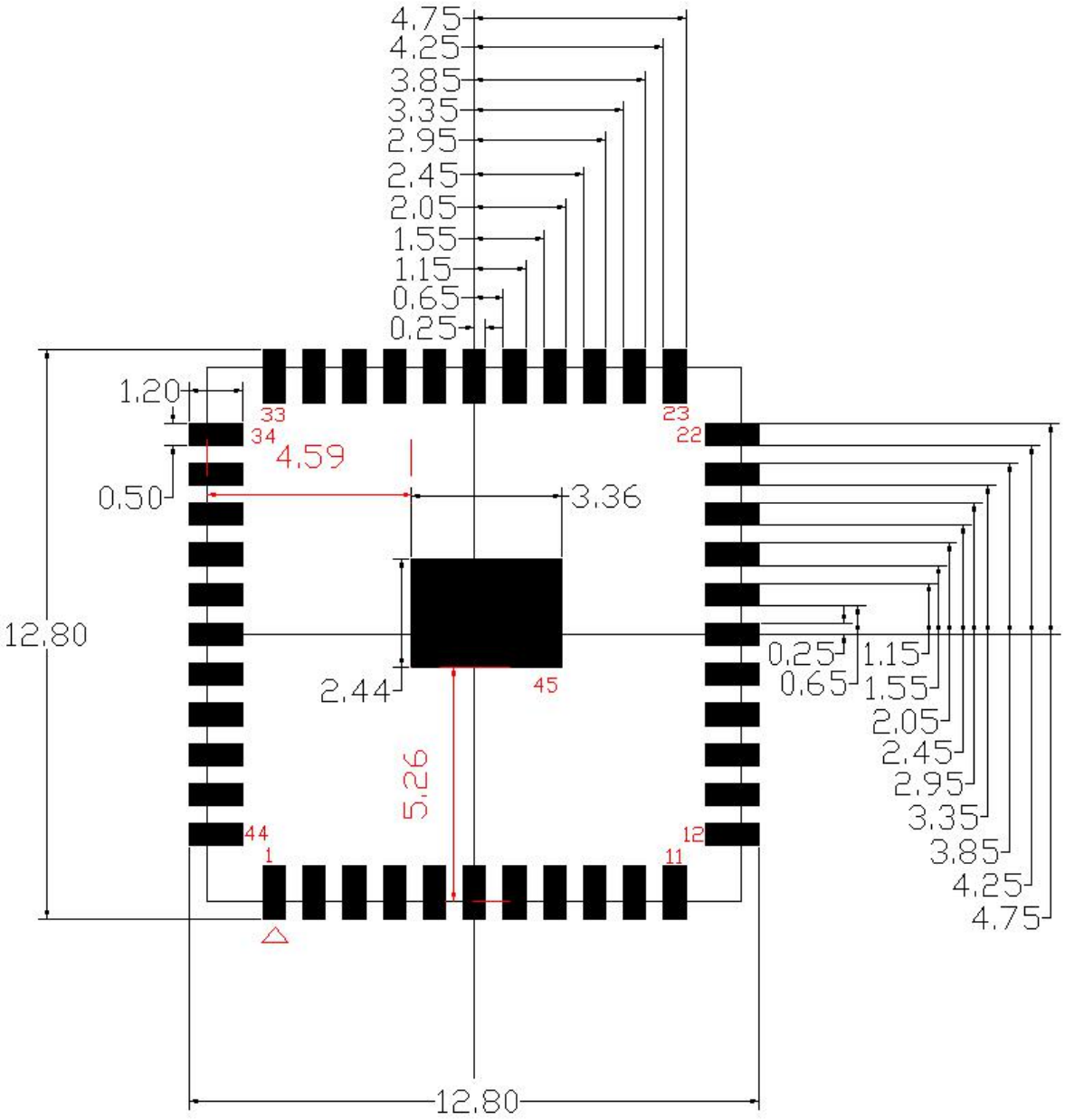


5.3 Physical Dimensions

<TOP View>


12.00
10.40
4.75
4.25
3.85
3.35
2.95
2.45
2.05
1.55
1.15
0.40
0.65
0.25
0.80
0.50
33
34
23
22
3.36
3.79
10.40
12.00
45
2.44
4.46
1.25
44
1
12
11
1.25
0.25
0.65
1.15
1.55
2.05
2.45
2.95
3.35
3.85
4.25
4.75

5.4 Layout Recommendation



6 Host Interface Timing Diagram

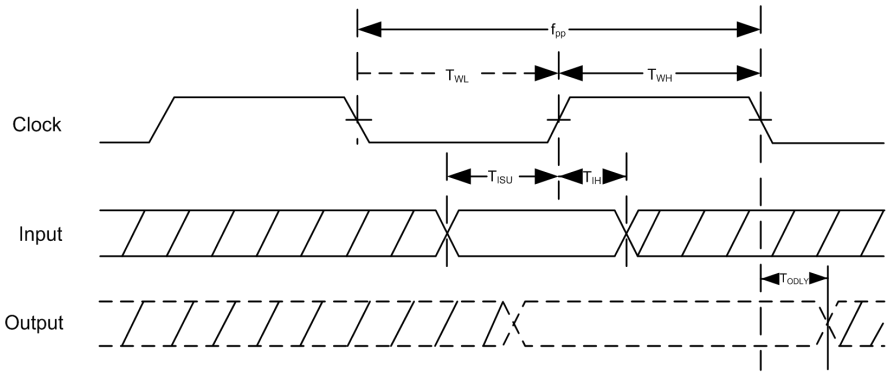
6.1 SDIO Pin Description

The module supports SDIO v2.0 signal level ranges form 1.8V to 3.3V.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

6.2 SDIO Default Mode Timing Diagram

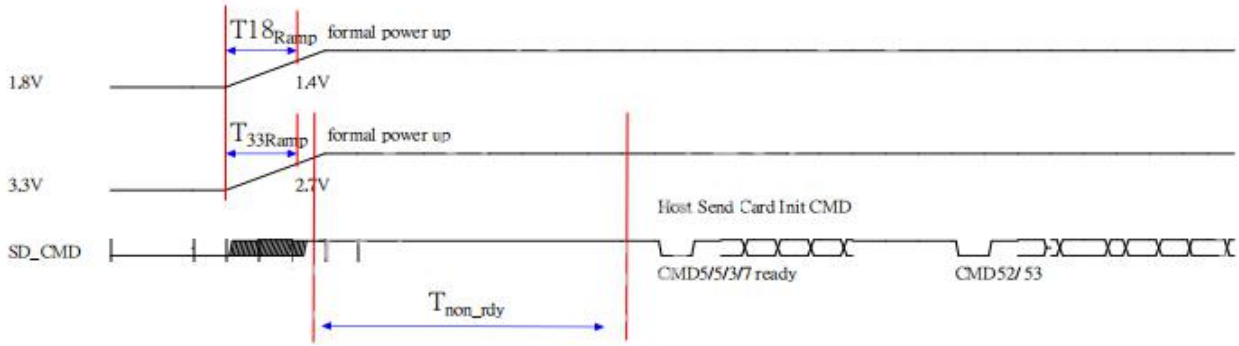


SDIO Interface Timing

SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{pp}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

6.3 SDIO Power-on sequence



Symbol	Description
T_{33ramp}	The 3.3V main power ramp up duration.
T_{18ramp}	The 1.8V main power ramp up duration.
T_{non_rdy}	SDIO Not Ready Duration. In this state, the RTL8723DS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

Recommend the card detection procedures are dvided into to phass:A 3.3V powe pre-carge phase and a formal power up phase.

After main 3.3v ramp up and 1.8v ramp up, the power managemnt unit is enabled by the power ready detection circuit. The power management unit enable the sdio block.efuse is then autoloaded to sdio circuit during the Tnon_rdy duration. After CMD5/5/3/7 procedures, card detection is executed. When the driver hs loarded,normal CMD52 and CMD53 are used.

	Min	Typical	Max	Unit
T33ramp	0.2	0.5	2.5	ms
T18ramp	0.2	0.5	2.5	ms
Tnon-rdy	1	2	10	ms

6.4 PCM interafce

Symbol	Type	Pin NO	Description
PCM IN	I	27	PCM data input
PCM OUT	O	25	PCM data output
PCM SYNC	O	28	PCM synchronization control
PCM CLK	IO	26	PCM Clock

Module supports a PCM digital audio interface that is used for transmitting digital audio/voice data to /from the audio codec.Features are supported as below:

. Support Master and slave mode

. Programmable long/short Frame sync

. Support 8-bit A-law/u-law, and 13/16-bit linear PCM format

. Support sign-extension and zero-padding for 8-bit and 13-bit samples

. Support padding of audio gain to 13-bit samples

. PCM master clock output:64,128,256,or512KHz

. Supports SCO/ESCO link

6.5 UART interafce

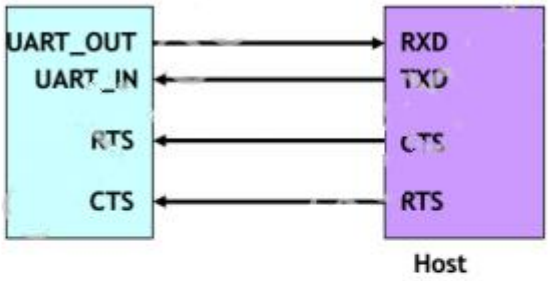
Below shown the UART hci interface connection guide.

Uart signal level ranges from 1.8V to 3.3V. must meet with the VDDIO voltage level.

HCI 硬件流程控制管脚连接

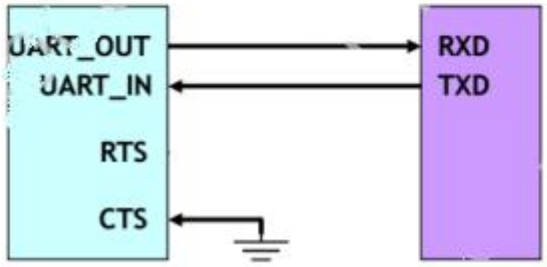
■ Host 有支持硬件流程控制的接法

圖(一)

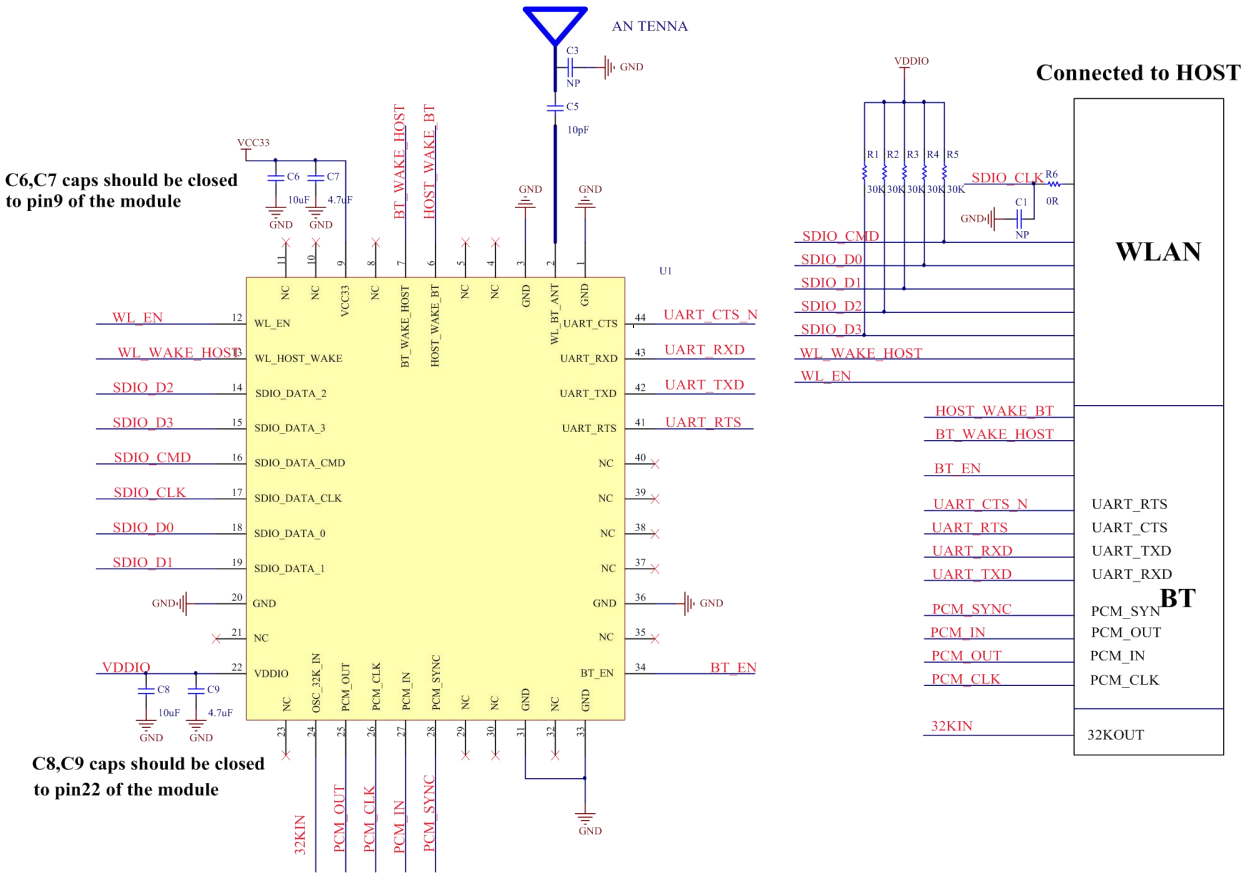


■ Host 不支持硬件流程控制的接法

圖(二)



7 Reference Design



8 Ordering Information

Part No.	Description
FG6223ASRD-W4	RTL8723DS, b/g/n, Wi-Fi BLE4.2, 1T1R, 12X12mm, SDIO/ Uart, PCB version V2.0, with shielding,DC-DC type

9 The Key Material List

Chipset	RTL8723DS-CG QFN48 4.4X4.4mm	Realtek
PCB	6223A-SRD 12X12X0.6mm 4L	XY-PCB,KX-PCB,SL-PCB ,Sunlord
Crystal	2520 24MHz 12pF 10ppm	TST,HOSONIC,TKD,ECE C,JWT
Inductor	0603 4.7uH ,±20%，>500mA	Microgate,sunlord,cenke,c eaiya

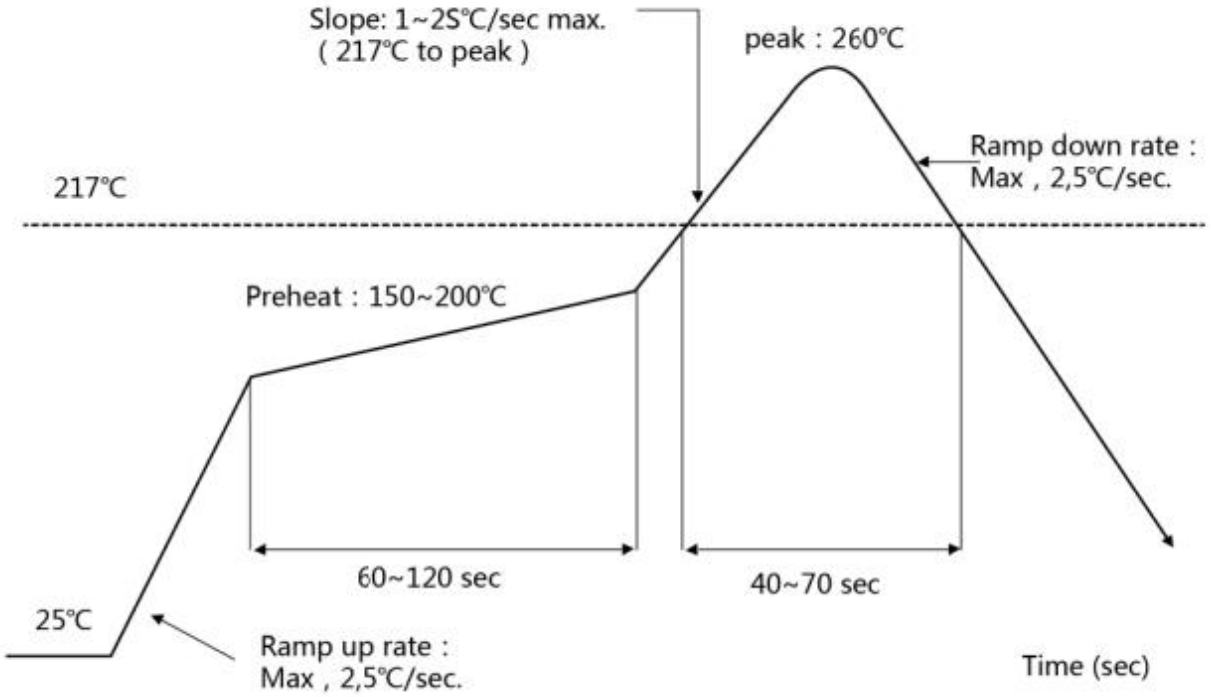
Shielding	6223A-SRD shielding	信太,精力通

10 Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

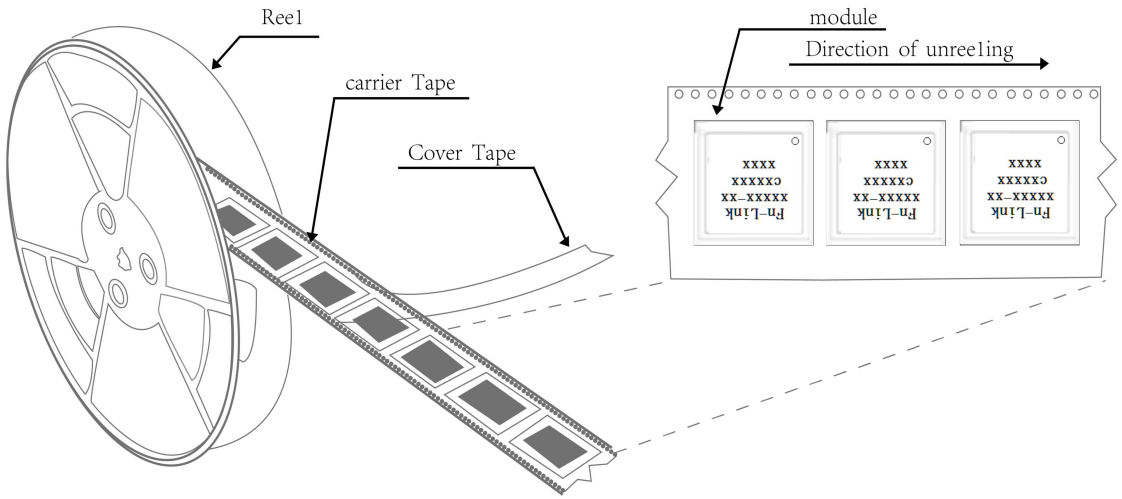
Number of Times : ≤2 times



11 Package

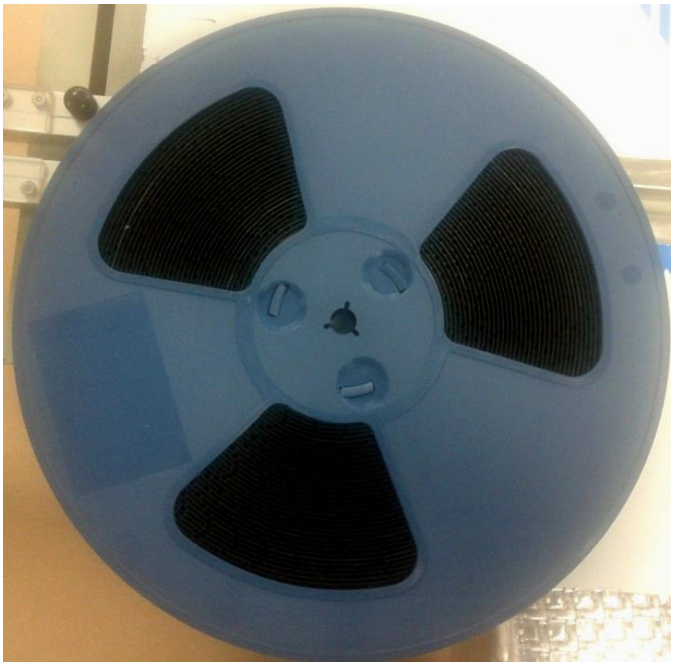
11.1 Reel

A roll of 1500pcs



11.2 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape :21.3mm*32.6m

Color of plastic disc: blue

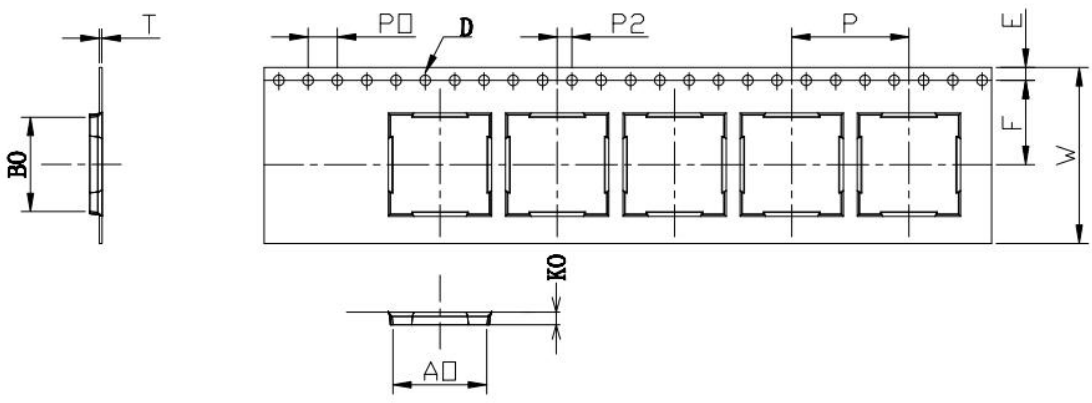
NY bag size:460mm*385mm

size ： 350*350*35mm

The packing case size:350*210*370mm

11.3 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	12.45	12.45	1.50	11.5	1.75	2.60	4.0	2.0	16.0	0.30
TOLE	+0.3 −0.3	±0.10	±0.10	+0.1 −0.0	+0.1 −0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



11.4 Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:
a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more